Fast and Accurate Packet Delivery Estimation based on DSSS Chip Errors

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Abstract—**Fast and accurate link quality estimation is an important feature for wireless protocols such as routing, rate switching or handover. Existing signal strength based estimators tend to be fast but inaccurate while packet statistic based approaches are more accurate but require longer estimation times. We propose a new link quality estimation approach based on chip errors in symbols for direct sequence spread spectrum transceivers. The new link quality estimator is evaluated experimentally with software defined radios on IEEE 802.15.4 for different link conditions, including multi-path and mobile scenarios. We show that our chip error based link quality estimator performs more accurately than received signal strength based estimators and much faster than the packet statistic based estimators with comparable accuracy. With our approach, only a single packet, or even a fraction of a packet (e.g., only a few symbols), is necessary to obtain similar performance as state-of-the-art approaches that require at least 10 packets.**

I. Introduction

Wireless networks heavily depend on packet delivery estimators to efficiently coordinate communication among devices. Routing, rate selection, and handover protocols are all example that require a quick and accurate estimation of the packet delivery in order to optimally schedule transmissions. Estimating the effective packet delivery in real world wireless networks proves however to be quite a challenging task. The unpredictable and location-sensitive nature of the wireless channels caused by effects such as mobility, fading or interference makes a theoretical treatment of the problem almost intractable.

Therefore in practice, packet delivery is almost always estimated using models relying on historical packet-level measurements. Such models rely either on (i) the received signal strength indicator (RSSI), (ii) packet delivery statistics, or (iii) a combination of both. RSSI-based models tend to be fast but researchers have found that they often fail to accurately predict the packet delivery in fading channels [1], [2], [3] as the correlation between both can be low. Packet statistics such as the ratio of successful transmissions provide a more accurate representation of the channel conditions and have shown to be more accurate than the RSSI based models [4], [5], [6]. However, these models are relatively slow as they require a few packets (>10 packets) for building up meaningful packet statistics. Hybrid models combining the above approaches [7], [8], [9] have shown to further improve the accuracy. Yet, the estimation time remains high as a few packets are still required to build up a reliable estimation.

In this paper, we explore the feasibility of modeling packet delivery using measurements from chip errors at the physical layer. Chips are the smallest unit of transmitted data and represent coded bits of information in direct sequence spread spectrum systems. We will consider IEEE 802.15.4 communication where four bits (one symbol) are represented as a sequence of 32 chips. Since many more chips are sent than packets per time unit, we expect a huge increase in time for the estimation of the packet reception ratio (PRR) due to the much higher sampling rate of the wireless channel. Eventually, we want to be able to estimate accurately the PRR based on a single packet or even just a fraction of the packet (e.g., only a few symbols).

Our major contribution is to demonstrate that we can effectively and accurately predict PRR in IEEE 802.15.4 using chip error statistics. In the next Section, we review state-of-the-art estimators. In Section III, we describe the basis of IEEE 802.15.4 and introduce our testbed and measurement setup. In Section IV, we analyze the chip and symbol error patterns for various link conditions (static vs. mobile, line-of-sight vs. non-line-of-sight). The use of software defined radios allows us getting various insights on the chip error patterns, as the demodulation and despreading is implemented in software. Based on our observations reported in Section V, we derive CEPS, a PRR estimator that relies on chip errors. In Section VI, we compare empirically the performance of CEPS with RSSI, packet statistics based and hybrid models and show that our approach manages to compete with packet statistics based models in terms of accuracy, while achieving estimation in just a fraction of the time of a single packet.

II. Related Work

Signal power based estimation. Modern IEEE 802.15.4 radio chips such as the Chipcon CC2420 report the RSSI and the link quality indicator (LQI). While these metrics have shown to be successful at quickly discriminating bad links from good ones, relating these indicators directly to the packet reception rate has shown to have inadequate accuracy under various channel conditions [1], [2], [10]. The authors of [3] use measurements from channel state information (CSI) to predict whether OFDM and MIMO links will deliver packets. In contrast, our work focuses on a DSSS system.

Packet statistics based estimation. Various link metrics that rely on packet statistics have been proposed in the literature. The Expected Transmission Count (ETX) [5] approximates the required number of retransmissions to successfully deliver a packet. The Window Mean Exponential Weighted Moving Average (WMEWMA) [4] uses an exponential weighted moving average filter to combine recently and previously measured packet reception estimates. RNP [6] counts the required number of packet transmissions and retransmissions before a successful reception. These metrics have been used

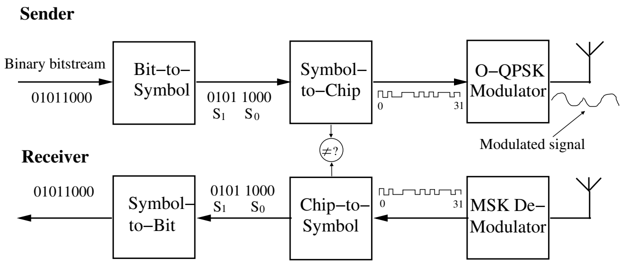

Fig. 1. Modulation and spreading functions in IEEE 802.15.4 [11].

mostly in static networks where the links are relatively stable over short times. Since they require a few packets to determine the delivery probabilities (usually above 10), packet statistics are not well suited for fast link estimation with low channel coherence time as for instance in mobile environments.

Hybrid estimation. Hybrid estimators combine signal power information (RSSI or LQI) and packet statistics to cope with weaknesses of single metrics. Fourbit [7] relies on converged information from the physical, link and network layers. The Fuzzy Link Quality Estimator [8] combines four link quality properties namely packet delivery, asymmetry level, stability factor, and SNR. The triangle metric [9] is a metric that combines geometrically the information of PRR, LQI and SNR into an hybrid estimator. While hybrid estimators tend to be more accurate than approaches that rely only on signal power or packet statistics, they still require a few packets for the packet statistics analysis.

III. Experimental Setup

The experimental setup in which we conduct our experiments is described below. We perform measurements (i) to gain an understanding of chip error patterns under various environmental conditions, (ii) as input for our PRR estimator, and (iii) to evaluate the accuracy of our metric.

A. 802.15.4 Background

IEEE 802.15.4 specifies a direct sequence spread spectrum (DSSS) system that is also adopted in IEEE 802.11b. DSSS spreads a low rate sequence of information bits to higher rate sequence of so called chips. In IEEE 802.15.4, this is achieved by a sender mapping a series of fours bits of data (later referred to as a symbol) to a sequence of 32 chips. The standard specifies the mapping of 16 possible data symbols to a predefined table of 16 chip sequences. At the sender side, the chip sequence is O-QPSK modulated to a baseband transmission waveform and ultimately transmitted over the air (see Fig. 1). At the receiver side, the signal is first demodulated using O-QPSK or minimum shift keying (MSK) as O-QPSK modulation with half-sine pulse shape is equivalent to MSK [12]. A correlator is then responsible for decoding the received 32 chip sequences to corresponding symbols. The received chips may be wrong. In order to map the chip sequences back to the original sent symbols, the receiver chooses the best matching symbol i.e., the closest 32 chip sequence defined in the IEEE 802.15.4 standard to the received one (e.g., in terms of hamming distance). However if too many chips are corrupted, the best-match at the receiver may be interpreted as a wrong symbol and the packet CRC will be wrong. For a more complete description, please refer to the standard [11].

B. Hardware and Software Platform

In order to gain access to low-level chip and symbol error information, we use GNU Radio software defined radios (SDR) running on commodity notebooks connected to Universal Software Radio Peripheral (USRP2) via the Ethernet interface. The USRP2s are equipped with a RFX2400 daughterboard that can deal with the 2.4 GHz frequency band of IEEE802.15.4. We rely on the IEEE 802.15.4 UCLA ZigBee [12], [13] code which we modify for the purpose of logging chip errors and compute different link quality estimators. The symbol-to-chip and chip-to-symbol boxes in Fig. 1 illustrate where we tap chip-level information. In our experiments, we generate synthetic traffic using iperf. The traffic consists of unidirectional 45 Bytes UDP packets sent at 10 Kbit/s. For each experiment run, we send 10,000 packets.

C. Scenarios

To capture the effects of different channel conditions such as fading, shadowing, or mobility on PRR estimation, we setup different testbed configurations to represent various types of connectivity. We consider nodes communicating over (i) attenuated cable, (ii) indoor line-of-sight (LOS), (iii) indoor non-line-of-sight (NLOS), (iv) outdoor line-of-sight, (v) and outdoor mobile links. In the wireless scenarios, nodes communicate over omnidirectional antennas. Exept in scenario (v), all nodes are static. In scenario (v), the mobile sender is moved on a tray back and forth approximately 8m passing by the receiver each time. During each measurement run of 10,000 packets we could create 20 sequences of approaching and moving away from the fixed receiver.

IV. Chip Error Pattern Analysis

This section analyses the chip error patterns we observed in the different scenarios. The insights of this analysis will serve as the basis for the development of the PRR estimator based on chip errors in the next section.

A. Distribution of Chip Errors

In a first step, we study whether chip errors tend to be more probable at particular positions in symbols. To measure the chip errors, we send known symbols that we analyze at the receiver by matching the transmitted chip sequences with the received ones. Our results show that the position of chip errors within individual symbols are equally probable for all chip positions, and this is consistent in all scenarios. Concerning the chip error distribution in symbols over entire packets, we observed an increased number of chip errors at the beginning (mostly caused by sychronization failures) and the end in the CRC fields. However, the chip error distribution over the symbols in the payload of packets proved to be uniform over all scenarios.

One of the key question is whether and how the chip errors correlate with the PRR. To answer this question we have determined the number of chip errors per symbol for

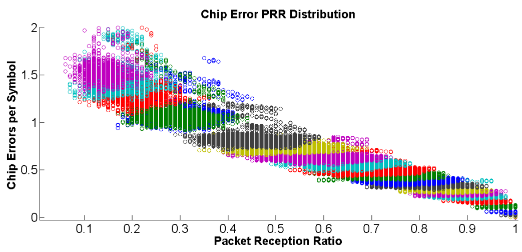

Fig. 2. PRR - chip error correlation (indoor line-of-sight).

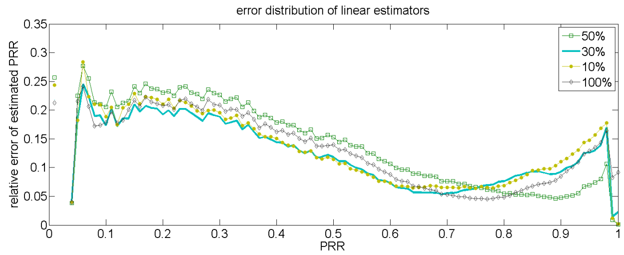

Fig. 3. PRR estimation error for different percentages of symbols used with most chips errors.

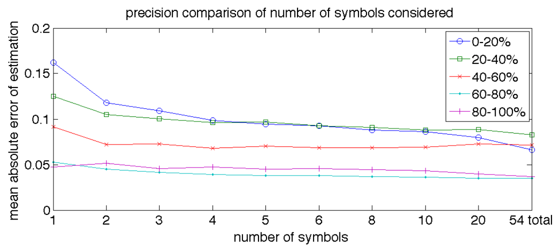

Fig. 4. PRR estimation error depending on the number of consecutive symbols used to determine CEPS.

the whole range of PRR values between zero and one in all scenarios individually. To estimate the real PRR, we averaged the measured PRR in scenarios (i) - (iv) over a window size of 100 packets around the packet where we measure the chip errors in symbols. Only the symbols from the payload are considered. Fig. 2 shows the result for the attenuated cable scenario (i). The different colors (or shades of grey) represent different measurement runs conducted for fixed settings of transmit power. We have omitted the plots for the other scenarios due to space constraints as they exhibit a similar pattern. We make two interesting observations. First, there is a clear correlation between the number of chip errors per symbol and the PRR: the higher the PRR, the lower the chip errors per symbol. We will use this correlation later to derive our chip error based estimator. Second, it might appear surprising that even links with a PRR below 10% do not exhibit more than 2 chip errors per symbol while in principle up to 32 chips could be erroneous (since 1 symbol=32 chips). After investigating this issue, we found out that too many chip errors in the preamble or start frame delimiter can prevent the receiver from synchronizing at all with incoming packets and those packets are thus simply ignored.

Additionaly, to determine if the burstiness of chip errors is a useful indicator for the PRR, we applied the β-factor of [14] to chips instead of packet losses. The β-factor assesses if losses happen in bursts or almost equally distributed based on conditional probability delivery functions. We did not found a way to correlate the chip β-factor to the PRR in an accurate form. We further tried to combine the chip β-factor with the chip errors per symbol in each packet but found no improvement over only using chip errors per symbol as a link quality indicator.

V. Chip Error Based Packet Delivery Estimation

As we saw in Fig. 2, the chip errors per symbol (CEPS) correlates nicely with the PRR. We therefore propose a simple model to quickly and accurately predict the packet delivery probability based on CEPS measurements.

A. Model Fitting: Geometric Linear Model

The linear correlation of the the chip error with the packet reception ratio can directly be exploited to build a geometric model drawn in the center of the scatter plot of Fig. 2. Pursuing this approach we get a model of the form

$$PRR_{CEPS} = \begin{cases} 0 & \text{if } \overline{CEPS} > Chiplimit, \\ 1 - \frac{\overline{CEPS}}{Chiplimit} & \text{if } 0 \leq \overline{CEPS} \leq Chiplimit. \end{cases}$$

We also considered a linear regression model to fit measurements but it is computationally expensive and locally biased where more data is available. We experimented extensively with both type of models and concluded that the geometric model is comparably accurate and thus dropped the idea of using a linear regression model. Relying on the geometric model, we fit the value $Chiplimit$ according to the measured data. $Chiplimit$ is the value where a simple linear model intersects with the CEPS axis and is on average approximately 1.7 in our experiments (see Fig. 2).

B. Averaging Chip Error Measurements

We investigate next how to effectively determine the average of the chip error per symbol $\overline{CEPS}$ to estimate the PRR.

1) Which symbols to choose?: CEPS is a metric with a potential range of 0 to 32. However, even for low quality links with PRR $\leq 20\%$, the average CEPS is rarely higher than 2 (see Fig. 2). The reason is that for low quality links, the transmission often fails to synchronize successfully in the first place, while if the synchronization is successful, the average CEPS tends to remain small. To improve this range and get a more pronounced distribution, we considered using only the symbols in the payload that exhibit the most chip errors. If we look at a cumulative distribution function of all the occuring realizations of the CEPS value in one sent packet, we take only a percentage containing the highest error values, e.g. the 10% symbols containing the most chip errors. The high value selection enables us to push the average error range of chip errors per symbol from $[0\ 1.7]$ to $[0\ 8.0]$. The deviations around the model however stay in the same range when considering only the worst symbols. As we see in Fig. 3, the precision of the resulting estimators only marginally improved or is, for some ranges of the PRR, even worse than when considering all symbols of the payload for the estimation.

2) How many symbols are needed?: An important parameter to optimize the speed of the PRR estimator is to evaluate the minimum number of symbols required to get a sufficiently precise estimate of the PRR. We therefore compare the evolution of the estimation error for an increasing number of considered symbols (starting at the beginning of the payload) for different ranges of PRR in 20% steps (i.e., 0-20%, 20-40%, ..., 80-100%) in scenarios (i)-(iv). Fig. 4 shows that already four symbols (i.e., 128 chips) provide an estimate in a range of 1% to the estimate generated considering the whole payload (54 symbols) and this is consistent for all PRR ranges. Only for channels with 0% <PRR< 20%, we see an improvement in precison of 3% for more than four symbols.

We conclude that small data packets or even a beacon as small as a few bytes are sufficient to estimate the packet reception ratio using our geometric model based on CEPS. This even applies for low quality links (PRR=0-20%). Our intuition that chips offer a high sampling rate of a link's quality, which can be mapped accurately to a PRR is confirmed. Furthermore, the estimation is not computationally expensive as it relies on a geometric model.

VI. Comparison with Existing PRR Estimators

This section compares our chip-based packet delivery estimator, CEPS, with metrics that rely on signal power, packet statistics, and hybrid approaches.

A. *Considered Estimators*

We consider the following estimators for comparison:
SNR. The implementation is based on the ASNR membership function of the Fuzzy LQE [8] and relies on SNR values reported for each received packet.
LQE. Inspired by hybrid metrics which combine signal power and packet statistics to improve performance, LQE combines chip error rate information with signal power.
ETX. ETX [5] relies solely on packet delivery statistics and is computed at the receiver side.
WMEWMA. The WMEWMA metric [4] is a filtered estimate of packet delivery statistics. The parameters of WMEWMA are set as in [4] and in the comparative simulation study by Baccour et. al. [15].
Four-Bit. Four-Bit [7] is a hybrid estimator that relies on converged information from the physical, link and network layers.

Tab. I provides further estimator details, reviews the number of packets each estimator requires to make a PRR estimation, and whether an estimator requires calibration. Except ETX and WMEWMA, all estimators require some kind of callibration to set the parameters according to the characteristics of the receiver.

B. *Results*

To evaluate the different metrics, we test their performance in the five different scenarios over a whole range of PRR link qualities. We collect iperf traces for each scenario and then make an offline trace-based emulation of the metrics. This reproducable approach allows a fair comparison without bias.

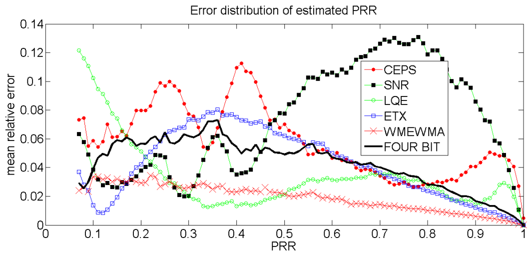

Fig. 5. Error distribution of different metrics in attenuated cable scenario.

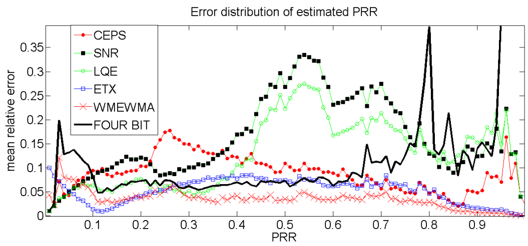

Fig. 6. Error distribution of different metrics in indoor LOS scenario.

1) Attenuated Cable Connection: Fig. 5 shows the PRR estimation errors of the different metrics for the attenuated cable connection. CEPS and LQE estimators keep up with the other estimators despite using only information gained from one packet. We observe as expected that the SNR estimator has the largest error but the relative error never tops 13% in the cable scenario. Best performing is the WMEWMA estimator as the cable connection is a very stable scenario. The PRR of this estimator is very precise and the error always below 4%. In general, we see that every estimator perfectly estimates the highest quality channels (PRR=1).

2) Indoor Line-of-Sight: From Fig. 6, we see the most significant changes compared to the cable connection. The error of the SNR metric increases significantly due to the more noisy environment which also affects LQE in a similar way. Somehow surprising, the Four-Bit estimator has problems

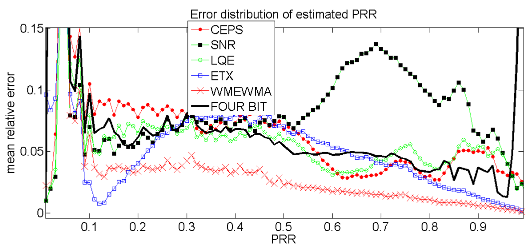

Fig. 7. Error distribution of different metrics in indoor NLOS scenario.

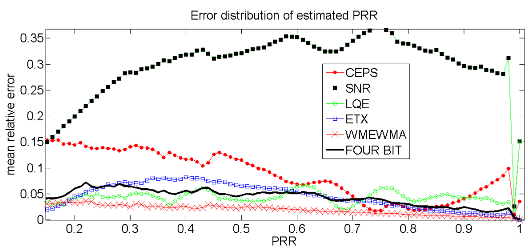

Fig. 8. Error distribution of different metrics in outdoor LOS scenario.

Estimator	Input	Formula	Parameters	Window Size (#Packets)	Cali-bration
CEPS	chip errors	$PRR_{CEPS} = \begin{cases} 0 & \text{if } \overline{CEPS} > Chiplimit, \\ 1 - \frac{\overline{CEPS}}{Chiplimit} & \text{if } 0 \leq \overline{CEPS} \leq Chiplimit. \end{cases}$	$Chiplimit = 1.7$	1	Yes
SNR	signal strength	$PRR_{SNR} = \begin{cases} 0 & \text{if } SNR < t_{lower}, \\ \frac{SNR - t_{lower}}{t_{upper} - t_{lower}} & \text{if } t_{lower} \leq SNR \leq t_{upper}, \\ 1 & \text{if } SNR > t_{upper}. \end{cases}$	t_{lower} = 26dB, t_{upper} = 34dB	1	Yes
LQE	hybrid (signal strength and chip errors)	same as above but with SNR replaced by $LQE = SNR - m * CEPS$	$m = 4$	1	Yes
ETX	packet statistics	$PRR_{ETX} = PRR_{forward} \times PRR_{backward}$	$PRR_{forward} = 1$	10	No
WMEWMA	packet statistics	$PRR_{WMEWMA} = \alpha \times WMEWMA + (1 - \alpha) \times PRR_{WMEWMA}$	$\alpha = 0.6$	≥ 10	No
Four-Bit	hybrid	$PRR_{FourBit} = \frac{1}{1+Four-Bit}$		≥ 5	Yes

TABLE I
OVERVIEW OF ESTIMATORS.

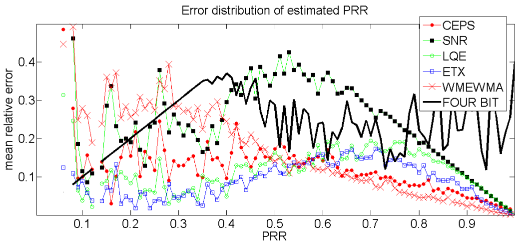

Fig. 9. Error distribution of different metrics in outdoor mobile scenario.

estimating the PRR of good channels which is due to the filtering of abrupt changes which happen to occur even when nodes are static. The CEPS metric performs well (except for some spikes) below an estimation error of 10% and follows closely the packet statistics based estimators.

3) Indoor Non-Line-of-Sight: From Fig. 7, we observe less distortion for the SNR and the LQE performance also becomes competitive again. The Four-Bit estimator performs better and the CEPS estimator is only outperformed by the WMEWMA metric while keeping the relative estimation error below 10%.

4) Outdoor Line-of-Sight: The SNR metric shows in Fig. 8 once more to be worst. CEPS is only half as precise as the packet statistics based metrics but the LQE metric remains competitive. Overall the packet statistics based estimators perform well (error $< 10\%$) over the whole range of PRR channel quality, which will be mostly due to the static conditions in the outdoor scenario with no changes in environment and almost no interfering radio signals from different sources.

5) Outdoor Mobile: The final scenario provides the most insights in order to evaluate the agility of the metrics as mobility comes into play. Fig. 9 clearly shows that in general, all metrics perform worse. For the first time, WMEWMA shows bigger problems caused by the fast changing low quality channels. The same applies for the highly history dependent Four-Bit estimator, which seems to have problems especially for channels resurrecting quickly from broken to perfect. CEPS displays similar performance as for the static scenarios despite some spikes for low quality links. The same is true for the LQE estimator which suffers from SNR precision problems for high quality channels.

VII. CONCLUSIONS

With a software defined radio based implementation of IEEE 802.15.4, we have shown experimentally that chip errors in packets serve as good indicator to predict a link's packet reception ratio (PRR). We have hence defined a fast and accurate link quality estimator based on the chip errors per symbol. Our approach proved to be more accurate than SNR based estimators especially in difficult channel conditions like mobile scenarios. Although our approach is slightly less accurate than state-of-the-art packet based estimators, it can estimate a link quality in only a few bytes of received data while others require several packets to get meaningful estimations. Even recent hybrid estimators relying on cross-layer optimization are still not capable of dealing with condition changes as fast as one packet. Our approach fills the time scale gap between link estimation based on received signal strength and packet statistic based estimation.

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